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Sapozhnikov V.V. (port.at.pgups1@gmail.com), **Sapozhnikov V.I.**, **Efanov D.V.**

Emperor Alexander I St. Petersburg state transport university

SYNTHESIS OF THE SELF-CHECKING CONTROL CIRCUITS FOR COMBINATIONAL LOGICAL DEVICES BASED ON THE BOOLEAN COMPLEMENT METHOD AND USING TWO-RAIL CHECKERS

The paper concentrates on the development of self-checking integrated control circuits synthesis theory, specifically on the Boolean complement method. The authors propose an algorithm of self-checking integrated control circuits synthesis, based on application of two-rail checkers as a device for verifying the accuracy of calculations. The algorithm takes into account the necessity to form a complete set of test combinations for the elements of addition by modulo two of the Boolean complement block and the two-rail checkers. The weaknesses of the algorithm and the method as a whole include the necessity to sort the Boolean complement options out to provide self-check and to decrease structural redundancy of the automation device. However, the method is universal and allows synthesizing self-checking integrated control circuits for automation devices implemented on any element base with structural redundancy less than in the situation of using duplication.

Keywords: self-checking integrated control circuit; Boolean complement; two-rail checkers; testability of elements.

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