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A SOFTWARE SUBSYSTEM FOR ACCEPTABILITY REGION ANALYSYS

Authors propose the method for synthesizing encoders for weight-based sum codes based on the decomposition of weight coefficients in powers of 2 and using standard circuits of full adders and half adders. The developed approach is proposed for use as the basis of multiplexers included in the logical cells structure of modern programmable logic integrated circuits. The possibilities of applying the developed method for synthesizing encoders for constructing structures of modular and modified weight-based sum codes are shown.

Keywords: weight-based code; encoder; full adder; half adder; multiplexer.

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